A very low power and low signal 5 bit 50 M samples/s double sampling pipelined ADC for Monolithic Active Pixel Sensors in high energy physics and biomedical imaging applications

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***Abstract*–The use of CMOS Monolithic Active Pixel Sensors (MAPS) for high precision minimum ionizing particle tracking has been proven to be a viable and powerful novel experimental technique. Possible applications will strongly depend on a successful implementation of on-chip hit recognition and sparsification schemes. For this aim, a 5 bit very low power and low level signal analog to digital converter (ADC) using a double sampling switched capacitor technique has been implemented in 0.35µm CMOS technology. A non-resetting sample and hold stage is integrated. This first stage compensates both the amplifier offset effect and the input common mode voltage fluctuations. The converter is composed of three successive 1.5 bit pipeline stages followed by a 2 bit flash stage. The prototype consists of 16 ADC double-channels; each one is sampling at 50 MS/s and dissipates only 1.38 mW at 2 V supply voltage. A bias pulsing stage is integrated in the circuit. Therefore, the analog part is switched OFF or ON in less than 1 µs. The size of the ADC is 80 µm × 1.4 mm. This corresponds to the pitch of 4 pixel columns in which each one is 20 µm wide and can be easily integrated in the MAPS.**

I. Introduction

CMOS Monolithic Active Pixel Sensors (MAPS) are charged particle tracking devices, integrating on the same silicon substrate radiation sensitive detector elements with its front-end readout electronics. Fabricated in standard CMOS technology, MAPS offer well known advantages like low power, low cost fabrication, high spatial resolution, flexibility, radiation hardness, compactness, random access and fast read-out. Compared to the existing detectors like Charge coupled Devices (CCD) or Hybrid pixel Detectors (HPD), MAPS are an attractive alternative to fulfill the requirements of Vertex Detector in the future high energy physics and biomedical imaging applications. However, the use of MAPS in different applications will strongly depend on a successful implementation of an on-chip read-out electronics. This is not a trivial task because of different constraints on the A/D converter design. The pixel signal is very low in the range of millivolts, which are the same order of magnitude as transistor threshold variations of a CMOS process. In order to obtain a high speed and a pixel level integration, the sampling rate is set at 10 M samples/s. The consumption of pixel column ADC must be less than 500 µW. The layout has to be adjusted to the small pixel pitch (20 µm × 20 µm).

In this paper, a 50 M samples/s double sampling analog to digital converter is described. It is designed according to the requirements of pixel arrays developed at IPHC-Strasbourg in collaboration with DAPNIA-Saclay, in perspective of the Linear Collider vertex detector [1], [2]. Figure 1 shows the global architecture of the planned MAPS chip comprising the pixel array with its associated read-out electronics and A/D conversion stages.

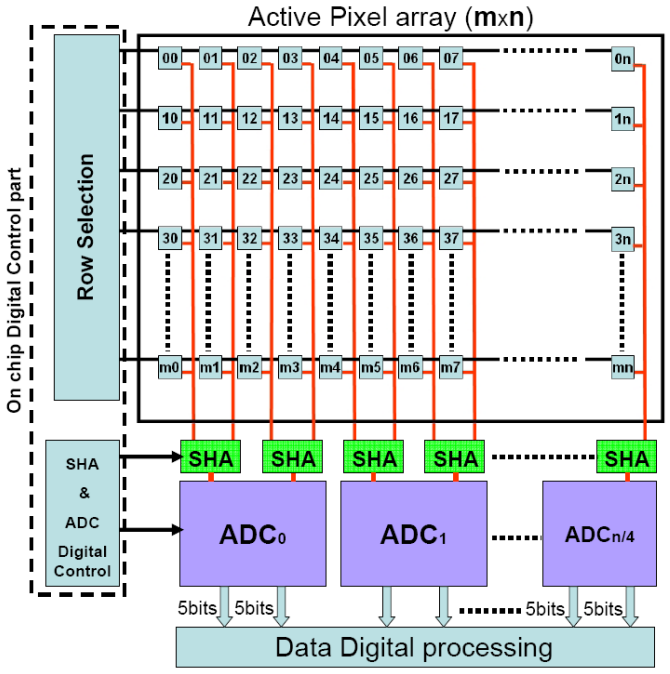

Fig. 1. Global architecture of MAPS and integrated readout electronics.

These MAPS are currently being developed and characterized at IPHC/Strasbourg in collaboration with CEA/Saclay and manufactured by TSMC through MOSIS [3], [4]. They are based on DC pixel architecture which comprises in-situ a first conditioning micro-circuit. Figure 2 shows a structure of an active pixel. When a particle (electron, photon…) traverses the pixel, it generates electron-hole pairs

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in the sensitive volume. The electrons are then collected by the n-well.

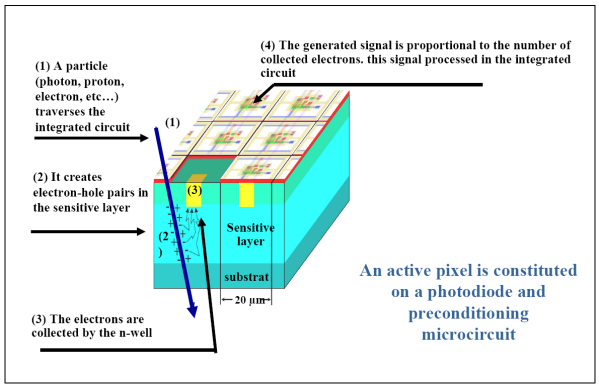

Fig. 2. Active pixel principle.

The charge is converted to voltage by the "pn" junction. The signal at the analog output of the pixel is the difference between a reference level (calibration) and the readout signal (read). This leads to the signal extraction and a reduction of the output pedestals (offsets). The pixel columns are read in parallel with a frequency in excess of 10 kHz. Thus, the pixel read out frequency is 10 MHz; this depends on the number of lines of the pixel matrix [3]. Each column is presently followed by a discriminator, which will be replaced in future by an ADC. In our application, each ADC converts 4 columns with an equivalent frequency of 10 M samples/s each column. The pixel column width amounts to 25 µm at present, but it should become 20 µm in the next prototypes.

II. DESIGN ARCHITECTURE

A Small size, a low power, a high speed and a high accuracy are the criteria which determine the ADC architecture to be chosen. A pipelined architecture provides a good deal between all these requirements. An overview block diagram of a 5 bit pipelined ADC is shown in figure 3 [5], [6] [7], [8]. The scheme includes 2 sample and hold circuits which compose the first stage of the design.

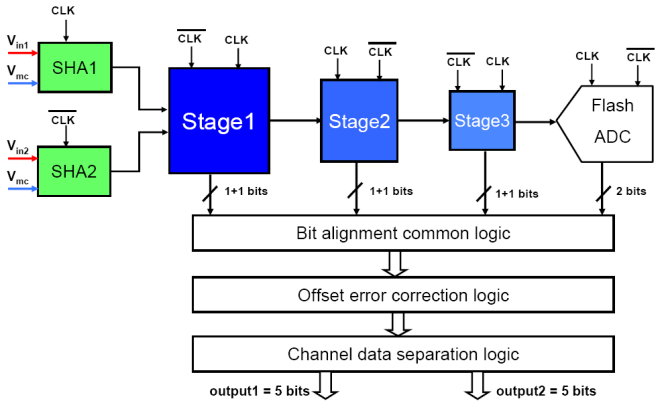

Fig. 3. General block diagram of a 5 bit pipelined converter.

A sample and hold amplifier (SHA) stage is needed to maintain the signal stable during the conversion time. The pixel common mode voltage fluctuation, the small value of the Least Significant Bit (LSB ~1mV) and the offset make the design of this first stage of the converter very critical. The SHA stage samples, holds and amplifies by 4 the analog input signal. It is followed by three successive 1.5 bit pipelined stages and a 2 bit flash stage. Each pipelined stage produces a digital estimate of an incoming held signal, then converts this estimate back to the analog, subtracts the result from the held input. This residue is then amplified before being transferred to the next stage. The last stage, which is a 2 bit flash ADC, determines the LSB. The successive digital results from the ADC stages are appropriately delayed throughout a bit alignment network. Then a digital error correction stage is added to leave room for the comparator offset correction. Therefore, the comparator constraints are relaxed and the power consumption is reduced.

The following sections describe each stage of this converter and some testing results will be presented.

III. THE SAMPLE AND HOLD AMPLIFIER CIRCUIT

A charge redistribution non-inverting architecture is used to design this stage [9]. Figure 4 illustrates the sampling phase (phi2 is ON). The intensity signal (Vin+) is stored onto the set of 4 sampling capacitors (C37...C40) and the common mode signal (Vin-) is stored onto the capacitors (C33…C36). Then during the HOLD phase (phi1 is ON), the charge is transferred to the feedback capacitor C23. This results to amplification by 4 of the differential signal between the reference (dark level) and the intensity level. Each capacitor unit in this scheme is 107 fF. These capacitor values are chosen in function of the surface limitation and kT/C noise factor.

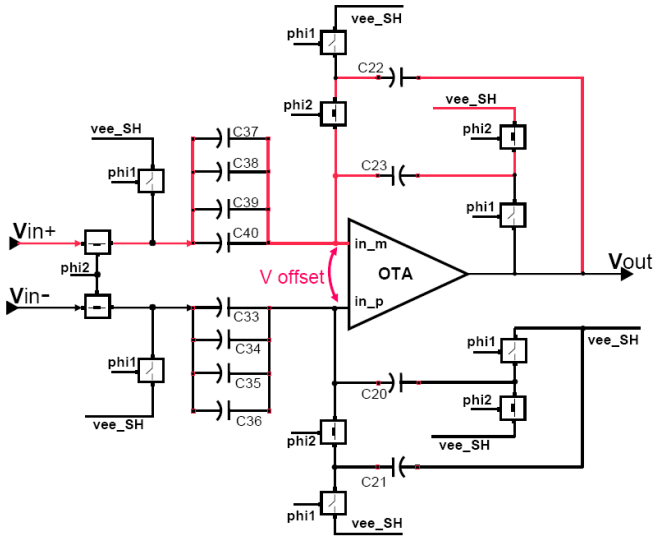

Fig. 4. Sample and hold amplifier scheme.

SHA1 and SHA2, as shown in figure 3, sample in opposite clock phases at 25 MHz frequency. So, the following ADC has a sampling rate of 50 MS/s which is performed by using the double sampling technique.

The particular requirements of the Vertex detector application make the design of the circuit very critical. The

restrictions in terms of power consumption and area make this design sensitive to different offset sources:

1. OTA input offset
2. Switch charge injection offset
3. Input common mode voltage fluctuation

The SHA stage has already been integrated and tested in our previous designs. The actual SHA is an improved version [8], [10].

A. *Design of the amplifier*

To design a high performance SHA, it is imperative to have an operational transconductance amplifier (OTA) of high gain-band-width (GBW) and fast settling behavior. Telescopic cascode architecture of the OTA is selected and implemented. The design of the OTA is shown in figure 5 [11]. This amplifier is used in both SHA stage and pipelined stages.

The current mirror load is a so called "wide swing cascode" [5]. It improves the dynamic range better than a basic cascode and makes the design robust for low voltage design. Bode diagram simulation results show that the amplifier achieves a 48.5 dB open loop gain and 160 MHz unity gain frequency with 75° phase margin. These results are obtained with a 1 pF load capacitance and 260 µW power dissipation at 2 V power supply.

A highest accuracy is needed in the first stage in order to achieve the required resolution of the ADC which follows. Keeping in mind this characteristics, the successive stages of the pipelined ADC use the same OTA architecture, but consume decreasingly (by a factor of 2) through the successive stages.

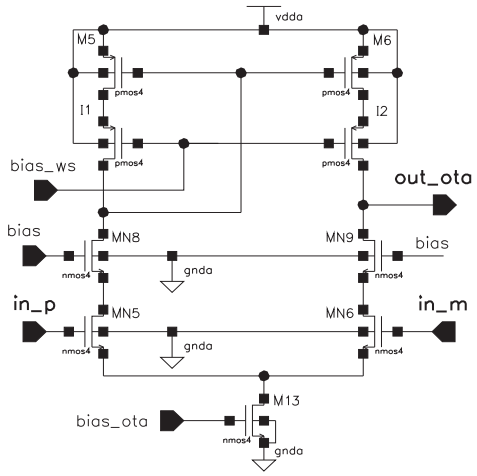

Fig. 5. A wide swing telescopic OTA.

IV. 5 BIT DOUBLE SAMPLING PIPELINED A/D CONVERTER

According to its well known performances, the pipeline architecture is selected to design the present ADC. The sample and hold stages of the ADC are designed using a switched capacitor technique.

The double sampling technique consists of sharing the active components between two adjacent ADC channels. In this section, each block of the design will be detailed. The double sampling design keys will be given. To have a better insight into the double sampling principle, traditional pipelined architecture is firstly described.

A. *1.5 bit pipelined stage implementation*

Figure 6 illustrates the implementation of a 1.5 bit pipeline stage. The A/D block consists of two comparators. The D/A conversion, subtraction, amplification, and S/H functions are performed by a switched capacitor circuit with a resolution of 1.5 bit per stage and an interstage gain of 2. Hence, the transfer function of this stage is $Vs = 2\times Vin - Vref_i$ where $Vref_i$ are the reference voltages selected by the DAC depending on the sub-ADC output code (b1b0).

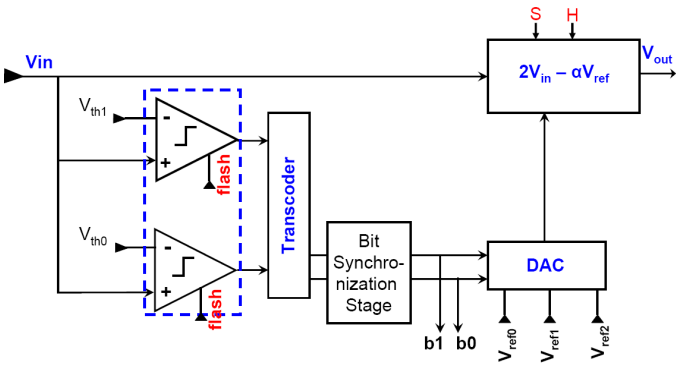

Fig. 6. Block diagram of 1.5 bit pipelined stage.

The characteristics of the transfer function for a 1.5 bit stage is shown in figure 7. The expression "1.5 bit" is used to indicate that only 3 combinations of the 4 are acceptable for the output codes. The (1, 1) code is avoided, thereby the interstage amplifier should not saturate and this leaves room for the digital error correction.

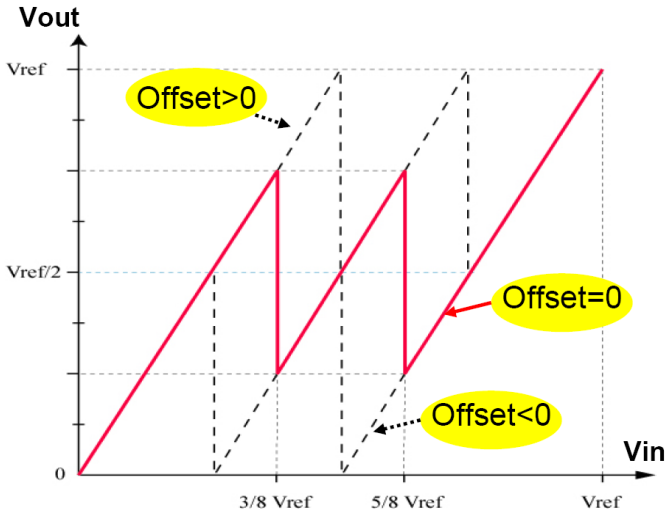

Fig. 7. A 1.5 bit residue transfer curve

The maximum comparator offset value tolerated is Vref/8 = ± 16 mV. Vref is the full range dynamic of this converter (Vref = 128 mV). A simplified schematic of the comparator is given in figure 8. It consists of a low gain and low offset

differential preamplifier followed by a latched folded cascode comparator to optimize the performance between the speed and the power consumption [12].

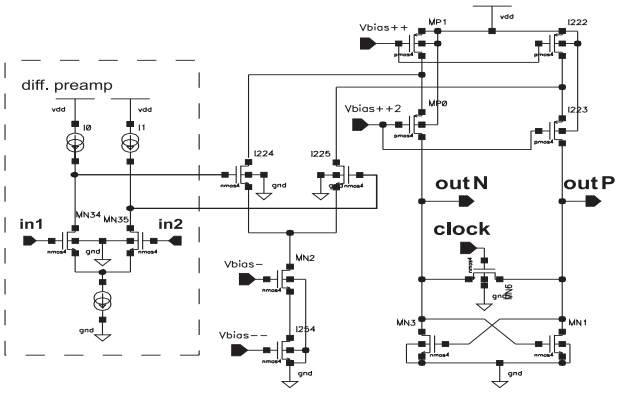

Fig. 8. Simplified comparator scheme.

The residue transfer curve is obtained by a precise multiplier sample and hold switched capacitor circuit shown in figure 9.

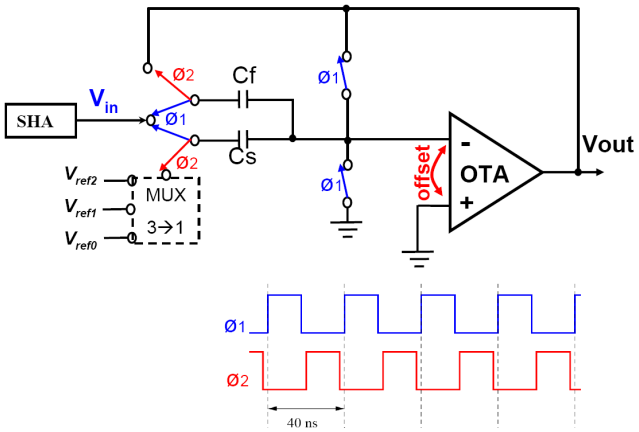

Fig. 9. The switched capacitor multiplier sample and hold scheme.

The incoming signal is sampled during phase "ø1". It is amplified by charge redistribution during phase "ø2". During the amplification phase, the bottom plate of the sampling capacitor (Cs) is connected to a reference voltage Vrefi which will be subtracted from the amplified signal. The residue values from this operation are transmitted to the next stage. The value for Vrefi is respectively *0, Vref/2 or Vref* depending on the comparator outputs (see figure 6). Vref is the dynamic range of the converter, with reference to the virtual ground.

B. Double sampling stage design

In the final design of the MAPS, at the bottom of each pixel column of the matrix there will be an ADC. So, the ADCs are disposed in parallel (figure 1). This feature can be exploited in the double sampling architecture [13].

The property of the successive ADC stages working in opposite clock phases can be exploited by sharing the operational amplifier, the comparators and the all the logic part between two parallel component ADCs. This approach uses the well known double-sampling concept of switched capacitor circuits. By using double-sampling, the equivalent sampling rate is doubled, but still the power dissipation remains almost the same as for an ADC having traditional single sampled pipeline stages with a half sample rate. The surface is reduced by ~ 40%. In contrast, the complexity of the pipeline stage is increased and more clock signals with different phases are needed.

Scheme of the double sampling multiplying D/A converter is shown in figure 10. The capacitors of two parallel channels working on opposite clock phases share the same amplifier. Due to the very low incoming signal, each ADC channel has its own SHA stage. While the "pipeline1" samples the Vin1 signal onto the Cs and Cf capacitors independently of the amplifier, the "pipeline2" switches to the amplification phase.

Two important side effects are caused by the amplifier sharing. First, the amplifier load capacitance is increased and affects its bandwidth. Second, the amplifier input offset is never reset; this can be tolerated by an adequate amplifier open loop DC-gain. The second one is very critical in this design because of the non differential architecture used here, and thereby no symmetric compensation is possible. Although algorithms of offset correction are available [14], but they are both area and power consuming. In this design, an auxiliary input is added to adjust manually the level of the common mode for each pipeline stage.

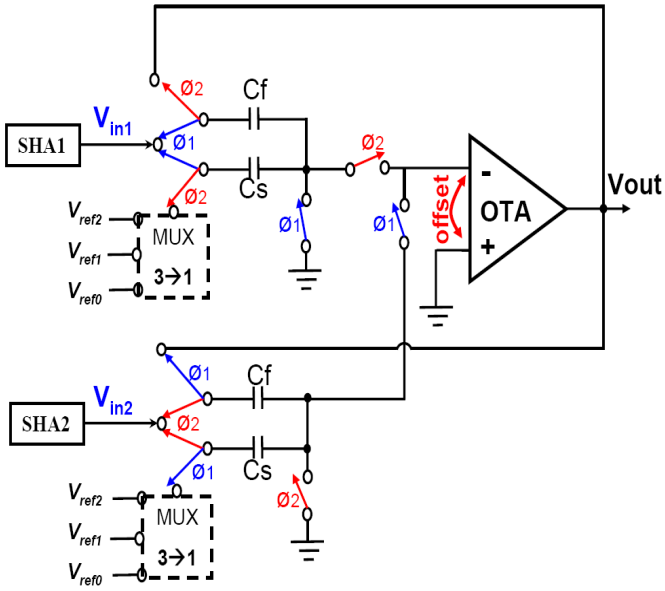

Fig. 10. A double sampling principle scheme.

C. Design limitations

The conversion speed is limited by the settling time of the operational amplifier used in the S/H circuits. The use of double sampling and parallelism introduces several limitations traduced by errors. These errors include offsets, gain and timing mismatches of the parallel channels. In this design the

threshold and reference voltages are generated out side of the prototype circuit. The large number of pipeline stages using the common reference voltages increases the capacitive load in the reference nodes. To guarantee that the reference does not limit the settling speed, its output impedance has to be very low (couple of tens of ohms).

V. TESTING RESULTS

A prototype has been designed in a CMOS 0.35µm process from Austria Micro System. It includes 16 channels of the described double sampling ADC. A photo of the chip is shown in figure 11. The dimensions of one full channel including the sample & hold amplifier stage are 80 µm × 1.4 mm. One may notice also that the surface occupied by the first stage (SHA) is about 1/4 of the full channel.

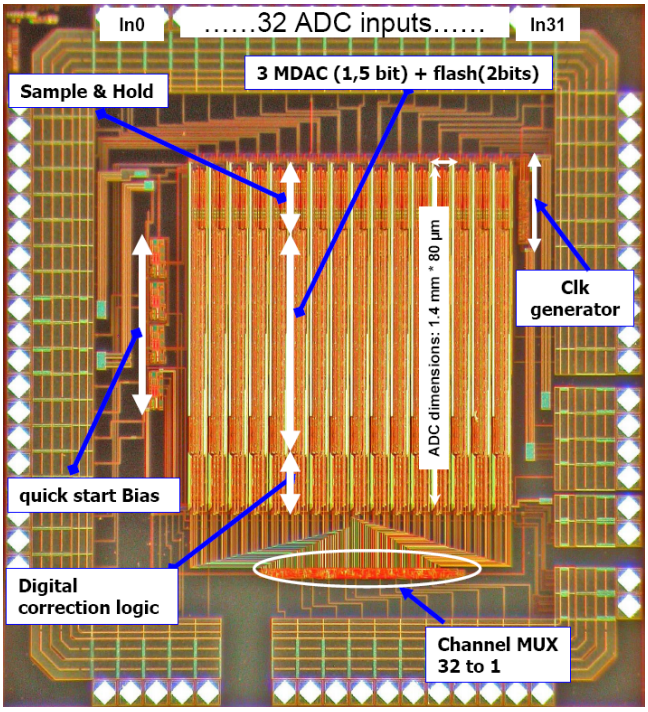

Fig. 11. Photo of the realized prototype.

The circuit has been tested successfully at 50 MHz; double-sampling concept is taken in count. In simulation, the ADC power dissipation at 2 V power supply is 0.69 mW this corresponds to the consumption of 2 pixel columns ADCs. But in the test, in order to compensate offsets, the power supply is set to 2.95 V. and consequently, the power dissipation is increased.

In figure 12 is shown the fast Fourier transform (FFT) spectrum for a 1 MHz sine wave input signal. The ADC achieves a dynamic range (SFDR) of 29 dB.

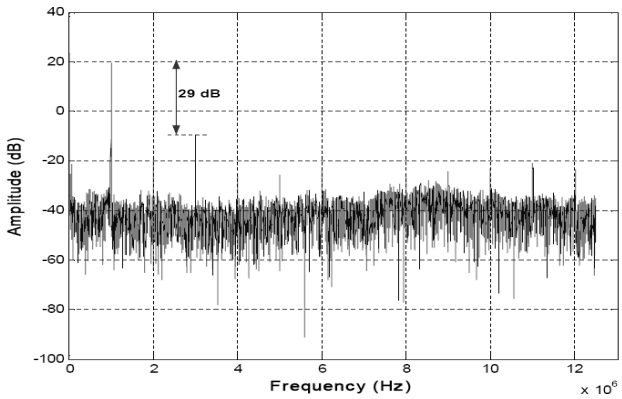

Fig. 12. FFT spectrum for a 1 MHz sine wave.

The dynamic study is done with Lab View signal analysis tools. The table 1 shows a summary of measured dynamic parameters.

TABLE I
ADC DYNAMIC PERFORMANCES

Fundamental frequency	1.00021 MHz
THD: total harmonic distortion	-27 dB
SINAD: signal-to-noise-and-distortion ratio	20.95 dB
SNR: signal-to-noise ratio	21.86 dB
SFDR: spurious-free dynamic range	29 dB

The converter output differential and integral nonlinearity errors (DNL, INL) are shown in figure 13.

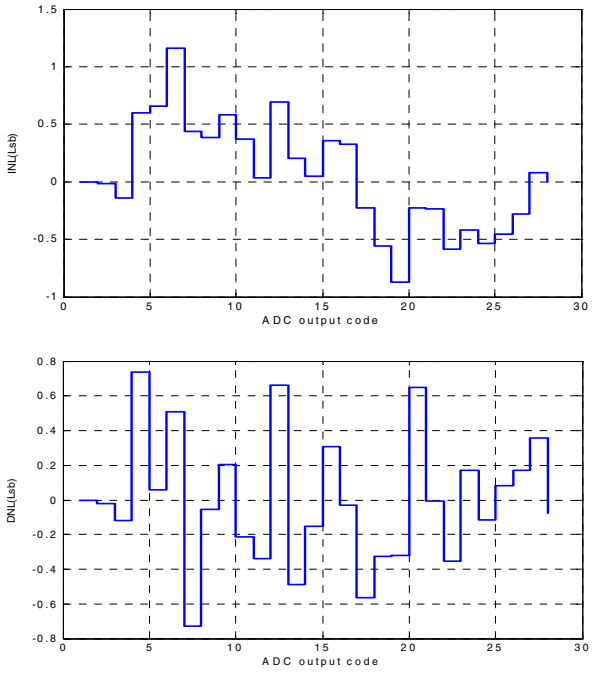

Fig. 13. DNL and INL results.

For this test, the input signal is a sine wave with a peak-to-peak amplitude close to the ADC full-scale range. Then a statistical analysis method is applied to the output data. A

maximum DNL error of 0.7 LSB and a maximum INL error of 1.2 LSB have been measured using a cumulative histogram method [15]. The DNL refers to the irregularity in the width of the quantization, while the INL quantifies the displacement of the transition levels from their nominal positions. Even if the INL and DNL errors are slightly superior to ½ LSB, no missing code is observed on the histogram of ADC out put code (figure 14). Theoretically to assure no missing code, the DNL and INL errors have to be less than ½ LSB [16].

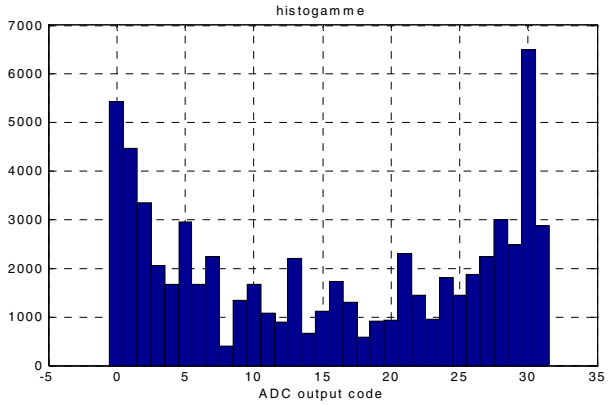

Fig. 14. ADC output histogram.

For the next ILC experiment, the beam duty cycle will be very low (~1%). It is therefore worthy to switch on the analog part of the circuit only when used, thus making the total power dissipation directly proportional to the beam duty cycle. This circuit includes such fast and efficient "power ON" capability. The analog bias settling and ADC wakening time result is given in figure 15. This bias pulsing circuit has already been integrated and tested in our precedent version of ADC [8], [10].

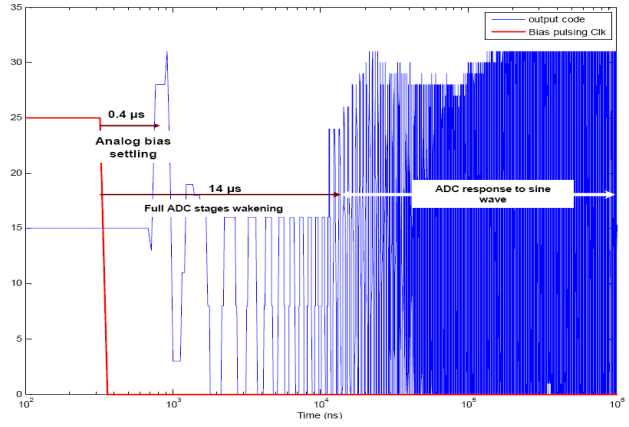

Fig. 15. Analog bias settling time and full ADC wakening results.

From the falling edge of a pulsing clock, the ADC begin to convert properly only after 14 µs. In the standby idle mode (pulsing clock at high level), the full analog part of the converter is switched OFF and the analog power dissipation is reduced to a ratio better than 1/1000. The characteristics of the design and some testing results are summarized in the table 2.

TABLE I I
ADC PERFORMANCE SUMMARY

	power Supply	Frequency (MHz)	Dimension (µm*µm)	INL (Lsb)	DNL (Lsb)	Power comsumption (mW)
test	•2.95 V analog •2 V digital	25	40*1400	Min: -0.8 Max: +1.2	Min: -0.7 Max: +0.7	3.42
Simulation	•2 V analog •2 V Digital	25	40*1400	0	0	0.69

VI. CONCLUSION

For Monolithic active pixel sensors, a 5 bit 50 MHz double-sampling A/D converter has been implemented in 0.35 µm CMOS technology. It achieves 29 dB of SFDR with a typical DC dissipation of 1.38 mW per 4 pixel columns; this corresponds to 0.35 mW/column. It is designed in perspective of the next linear collider (ILC). The full ADC includes an amplification sample and hold stage. A 1.5 bit/stage architecture is used for the converter in a non differential configuration. The size of one channel layout is 80 µm × 1.4 mm. A very efficient fast power pulsing is integrated with this circuit to reduce the total DC power dissipation according to the beam low duty cycle. Due to its high performances, this ADC can be widely used in high energy physics and biomedical imaging applications.

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